

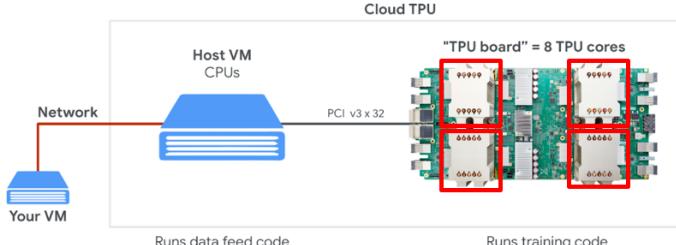
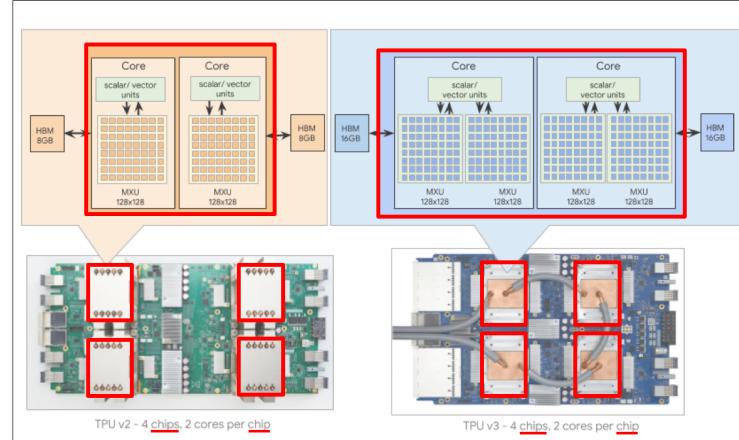
EXHIBIT D

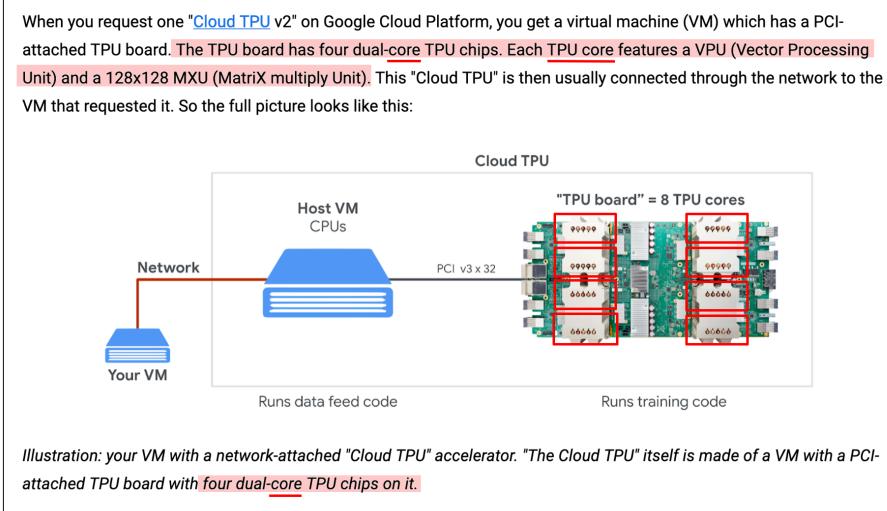
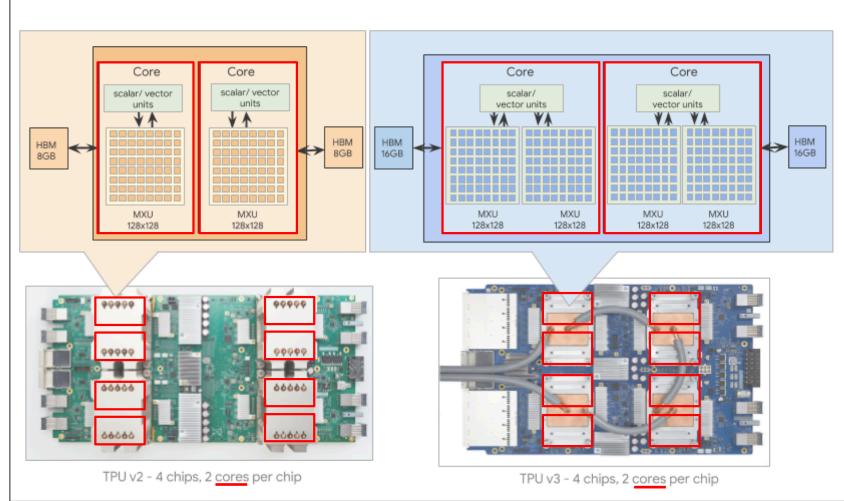
Exhibit B (Supplemental)

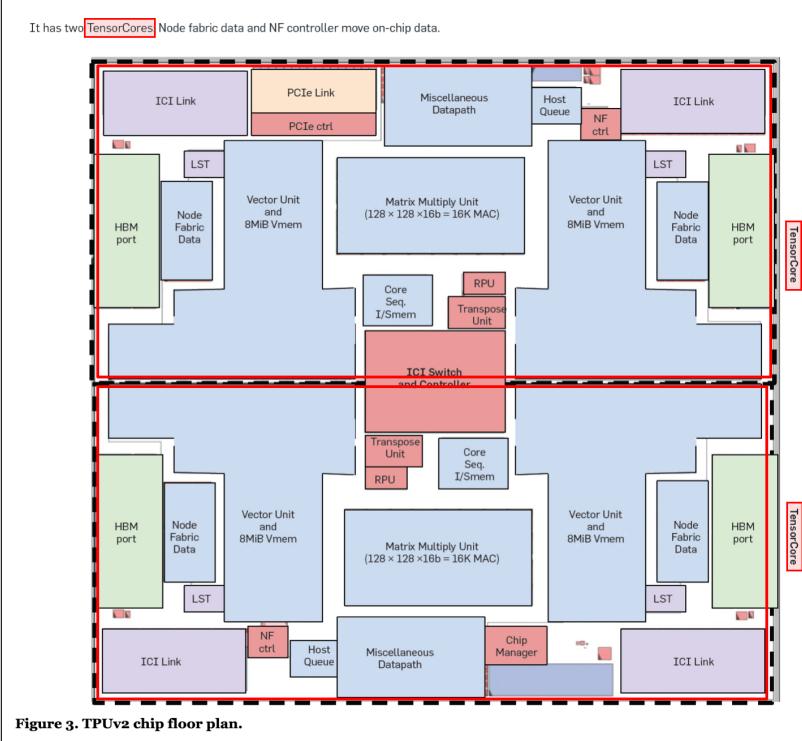
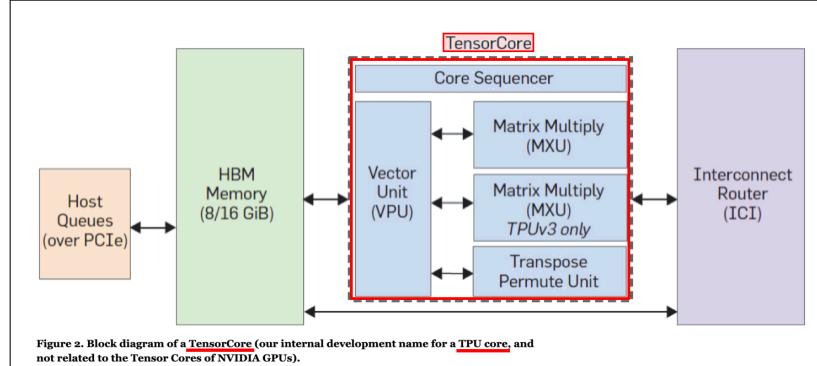
U.S. Pat. No. 8,407,273

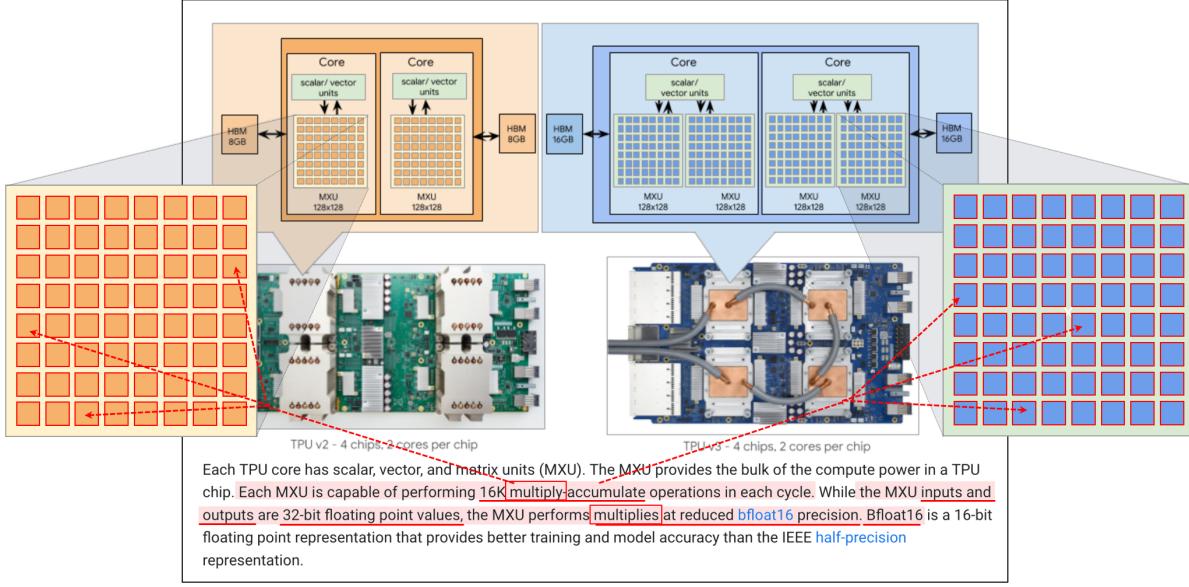
Claim 53

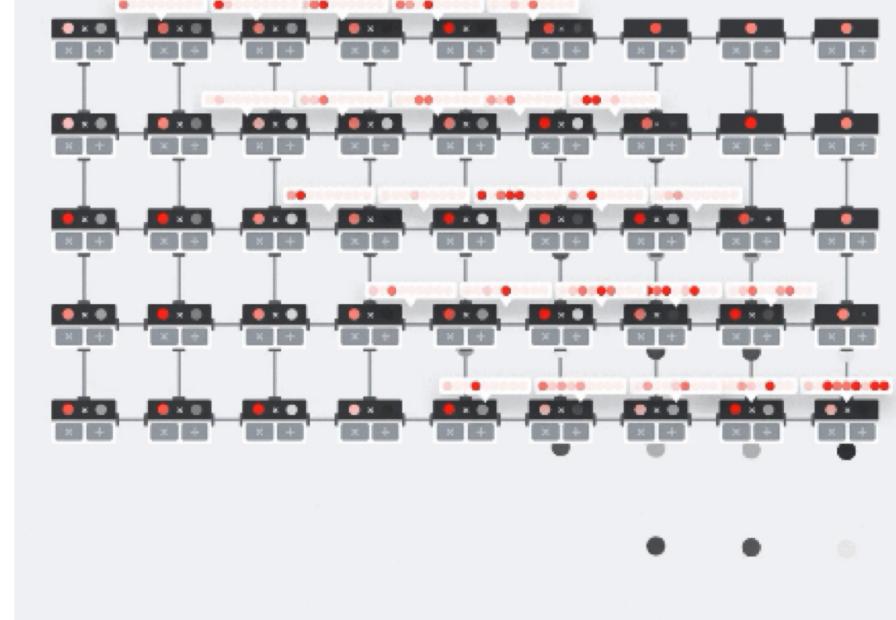
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As a side effect, the behavior of those processors can be difficult to predict, which makes it hard to guarantee a certain latency limit on neural network inference. In contrast, TPU design is strictly minimal and deterministic as it has to run only one task at a time: neural network prediction. You can see its simplicity in the floor plan of the TPU die.” https://cloud.google.com/blog/products/gcp/an-in-depth-look-at-googles-first-tensor-processing-unit-tpu (<i>emphasis in orig.</i>) “In mathematics, computer science and physics, a deterministic system is a system in which no randomness is involved in the development of future states of the system. A deterministic model will thus always produce the same output from a given starting condition or initial state.” https://en.wikipedia.org/wiki/Deterministic_system For each of the possible valid inputs to the multiplication operation performed by the multipliers within the MXU, Singular has computed the result and compared it to the result of an exact mathematical calculation performed on the same inputs. The results of this test showed that for more than 10% of the possible valid inputs, the numerical value represented by the output signal of each MXU multiplier differs by more than 0.2% from the result of an exact mathematical calculation performed on the same inputs. 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| float32 range: $\sim 1e^{-38}$ to $\sim 3e^{38}$ | S | E | E | E | E | E | E | E | M | M | M | M | M | M | M | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| float16 range: $\sim 5.9e^{-8}$ to $6.5e^4$ | S | E | E | E | E | M | M | M | M | M | M | M | M | M | M | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| '273 PATENT | SUPPLEMENTAL INFRINGEMENT EVIDENCE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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--|---|---|---|---------|
| <p>53. A device:</p> <p>comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,</p> <p>wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;</p> <p>wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.</p> | <p>The Accused Products independently meet this claim limitation for each “device” identified above:</p> <div style="border: 1px solid black; padding: 10px;"> <p>We cannot reveal technology details of our chip partner. Although it is in a larger, older technology, the TPUv2 die size is less than 3/4s of the GPU. TPUv3 is 6% larger in that same technology. TDP stands for Thermal Design Power. The Volta has 80 symmetric multiprocessors.</p> <table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Feature</th> <th>TPUv1</th> <th>TPUv2</th> <th>TPUv3</th> <th>Volta</th> </tr> </thead> <tbody> <tr> <td>Peak TeraFLOPS/Chip</td> <td>92 (8b int)</td> <td>46 (16b) 3 (32b)</td> <td>123 (16b) 4 (32b)</td> <td>125 (16b) 16 (32b)</td> </tr> <tr> <td>Network links x Gbits/s/Chip</td> <td>--</td> <td>4 x 496</td> <td>4 x 656</td> <td>6 x 200</td> </tr> <tr> <td>Max chips/supercomputer</td> <td>--</td> <td>256</td> <td>1024</td> <td>Varies</td> </tr> <tr> <td>Peak PetaFLOPS/supercomputer</td> <td>--</td> <td>11.8</td> <td>12.6</td> <td>Varies</td> </tr> <tr> <td>Bisection Terabits/supercomputer</td> <td>--</td> <td>15.9</td> <td>42.0</td> <td>Varies</td> </tr> <tr> <td>Clock Rate (MHz)</td> <td>700</td> <td>700</td> <td>940</td> <td>1530</td> </tr> <tr> <td>TDP (Watts)/Chip</td> <td>75</td> <td>280</td> <td>450</td> <td>450</td> </tr> <tr> <td>TDP (Kwatts)/supercomputer</td> <td>--</td> <td>124</td> <td>594</td> <td>Varies</td> </tr> <tr> <td>Die Size (mm²)</td> <td><331</td> <td><611</td> <td>>648</td> <td>815</td> </tr> <tr> <td>Chip Technology</td> <td>28nm</td> <td>>12nm</td> <td>>12nm</td> <td>12nm</td> </tr> <tr> <td>Memory size (on-/off-chip)</td> <td>28MIB/8GIB</td> <td>32MIB/16GIB</td> <td>32MIB/32GIB</td> <td>36MIB/32GIB</td> </tr> <tr> <td>Memory GB/s/Chip</td> <td>34</td> <td>700</td> <td>900</td> <td>900</td> </tr> <tr> <td><u>MXU/Cores</u></td> <td>1</td> <td>1 128x128</td> <td>2 128x128</td> <td>8 4x4</td> </tr> <tr> <td><u>MXU Size</u></td> <td>256x256</td> <td></td> <td></td> <td></td> </tr> <tr> <td><u>Cores/Chip</u></td> <td>1</td> <td>2</td> <td>2</td> <td>80</td> </tr> <tr> <td><u>Chips/CPU Host</u></td> <td>4</td> <td>4</td> <td>8</td> <td>8 or 16</td> </tr> </tbody> </table> </div> <p>Table 3. Key processor features.</p> <p>https://cacm.acm.org/magazines/2020/7/245702-a-domain-specific-supercomputer-for-training-deep-neural-networks/fulltext</p> <p>Norrie et al., “Google’s Training Chips Revealed: TPUv2 and TPUv3” (Presented at HotChips Conference, Aug. 2020)</p> <p>See also GOOG-SING-SC-000001-454.</p> | Feature | TPUv1 | TPUv2 | TPUv3 | Volta | Peak TeraFLOPS/Chip | 92 (8b int) | 46 (16b) 3 (32b) | 123 (16b) 4 (32b) | 125 (16b) 16 (32b) | Network links x Gbits/s/Chip | -- | 4 x 496 | 4 x 656 | 6 x 200 | Max chips/supercomputer | -- | 256 | 1024 | Varies | Peak PetaFLOPS/supercomputer | -- | 11.8 | 12.6 | Varies | Bisection Terabits/supercomputer | -- | 15.9 | 42.0 | Varies | Clock Rate (MHz) | 700 | 700 | 940 | 1530 | TDP (Watts)/Chip | 75 | 280 | 450 | 450 | TDP (Kwatts)/supercomputer | -- | 124 | 594 | Varies | Die Size (mm ²) | <331 | <611 | >648 | 815 | Chip Technology | 28nm | >12nm | >12nm | 12nm | Memory size (on-/off-chip) | 28MIB/8GIB | 32MIB/16GIB | 32MIB/32GIB | 36MIB/32GIB | Memory GB/s/Chip | 34 | 700 | 900 | 900 | <u>MXU/Cores</u> | 1 | 1 128x128 | 2 128x128 | 8 4x4 | <u>MXU Size</u> | 256x256 | | | | <u>Cores/Chip</u> | 1 | 2 | 2 | 80 | <u>Chips/CPU Host</u> | 4 | 4 | 8 | 8 or 16 |
| Feature | TPUv1 | TPUv2 | TPUv3 | Volta | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Peak TeraFLOPS/Chip | 92 (8b int) | 46 (16b) 3 (32b) | 123 (16b) 4 (32b) | 125 (16b) 16 (32b) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Network links x Gbits/s/Chip | -- | 4 x 496 | 4 x 656 | 6 x 200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Max chips/supercomputer | -- | 256 | 1024 | Varies | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Peak PetaFLOPS/supercomputer | -- | 11.8 | 12.6 | Varies | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bisection Terabits/supercomputer | -- | 15.9 | 42.0 | Varies | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Clock Rate (MHz) | 700 | 700 | 940 | 1530 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDP (Watts)/Chip | 75 | 280 | 450 | 450 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDP (Kwatts)/supercomputer | -- | 124 | 594 | Varies | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Size (mm ²) | <331 | <611 | >648 | 815 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Chip Technology | 28nm | >12nm | >12nm | 12nm | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Memory size (on-/off-chip) | 28MIB/8GIB | 32MIB/16GIB | 32MIB/32GIB | 36MIB/32GIB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Memory GB/s/Chip | 34 | 700 | 900 | 900 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>MXU/Cores</u> | 1 | 1 128x128 | 2 128x128 | 8 4x4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>MXU Size</u> | 256x256 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>Cores/Chip</u> | 1 | 2 | 2 | 80 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <u>Chips/CPU Host</u> | 4 | 4 | 8 | 8 or 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |